the interconnection of said first and second plurality of transistors providing an output adapted to be coupled to a load device;

a gate of one of said first plurality of transistors being adapted to receive a $\overline{\text{DOWN}}$ pulse signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive an UP pulse signal, and a gate of another one of said second plurality of transistors being adapted to receive another DC bias signal; and

cont'd C1

a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a DOWN pulse signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive an $\overline{\text{UP}}$ pulse signal.

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8. (Amended) A charge pump circuit comprising:

a first plurality of serially connected transistors of a first conductivity type;

a second plurality of serially connected transistors of a second conductivity type;

C2 said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors;

the interconnection of said first and second plurality of transistors providing an output adapted to be coupled to a load device;

a gate of one of said first plurality of transistors being adapted to receive a first switching signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive a second switching signal, and a gate of the other of said second plurality of transistors being adapted to receive another DC bias signal; and

a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a complementary first switching signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive a complementary second switching signal.

23. (Thrice Amended) A method of operating a charge pump comprising:

switching a first switching transistor in response to a first applied switching signal to affect an output at an output terminal adapted to be coupled to a load device;

switching a second switching transistor in response to a second applied switching signal to affect an output at said output terminal;

biasing the switching characteristics of said first and second switching transistors with bias transistors respectively serially connected to said first and second switching transistors;

coupling a complementary signal of said first applied switching signal to a connection between said first switching transistor and an associated bias transistor; and

coupling a complementary signal of said second applied switching signal to a connection between said second switching transistor and an associated bias transistor.

Please add new claims 25-29 as follows:

25. (New) A charge pump circuit as defined in claim 1 wherein said load device comprises a filter of a phase locked loop.

26. (New) A charge pump circuit as defined in claim 1 wherein said load device comprises an input of a voltage controlled oscillator.

27. (New) A charge pump circuit as defined in claim 1 wherein said first node is adapted to receive said Down pulse signal directly from a phase frequency detector.

contd C4

28. (New) A charge pump circuit as defined in claim 8 wherein said first switching signal is received directly from a phase frequency detector.

29. (New) A method of operating a charge pump as defined in claim 23 wherein said first applied switching signal is received directly from a phase frequency detector.